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132. An electronic system as claimed in claim 131 wherein the egress packet control defines the deadline interval Dj for an arriving packet j, having a sequence number Sj and frame width F, from a deadline Di of an earlier packet i having a sequence number Si, substantially as a function of frame width F and the difference of sequence numbers Sj and Si.

CONT

133. An electronic system as claimed in claim 131 wherein the egress packet control has stored instructions to preempt processing of the first received packet by preemptively processing the second received packet, when the deadline interval for the second received packet is less than the deadline interval respective to the first received packet by a predetermined amount.

134. An electronic system as claimed in claim 131 wherein the egress packet control has stored instructions for ingress packet processing, and for preempting egress packet processing of an egress packet having a deadline interval exceeding a value, by preemptively executing ingress packet processing of at least one ingress packet.

135. An electronic system as claimed in claim 131 having channel decoders that operate on non-coincident frame boundaries, and wherein if the second packet has a second deadline earlier than the first deadline, the egress packet control has stored instructions for testing to determine whether both the second and first packets can be decoded ahead of their respective deadlines, and if so, then preemptively executing decode of the second packet.

136. An electronic system as claimed in claim 131 whereas the egress packet control has stored instructions for the computing for each of said received packets respective deadline intervals as circular time differences between a respective deadline D and a respective packet arrival time A.